IN THE SPECIFICATION

Page 1, before the first line, add the paragraph:

--This is a continuation application of U.S. Serial No. 10/200,162, filed July 23, 2002; which is a continuation application of U.S. Serial No. 09/529,651, filed April 18, 2000, now U.S. Patent No. 6,499,663.--

Pages 15 and 16, the paragraph bridging these pages from page 15, line 22 to page 16, line 16, replace the bridging paragraph with:

The charge signal transferred from the horizontal transfer CCD unit 20 is converted to a voltage signal by a GCD type outputting unit 21. The outputting unit 21 has a floating capacitive element 23 coupled to the output node 22 of the horizontal transfer CCD unit 20, a precharge MOS transistor 24 for precharging the floating capacitive element 23 every cycle of the charge transfer by the pulse signals H1 and H2, and a source follower input MOS transistor 25 whose gate electrode is coupled to the output node 22. The source follower input MOS transistor 25 and a current source 26 construct a source follower output circuit and the source of the MOS transistor 25 serves as an output terminal 27. In Fig. 3, RG denotes a reset pulse; C0 the capacitance of the

floating capacitive element 23; C1 parasitic capacitance between the gate and source of the MOS transistor 24; C2 parasitic capacitance between the output node 22 of the horizontal transfer CCD unit 20 and the transfer gate which receives the transfer pulse signal H1; ~~and~~ C3 input gate capacitance of the MOS transistor 25; Vdd a power supply voltage; and Vss a ground voltage. The source follower output circuit of the outputting unit 21 is not limited to one stage. A plurality of stages may be connected in series.

Page 22, the second full paragraph, lines 15 to 23, replace the paragraph with:

The feedback clamping voltage generating circuit 33 has: a DAC 330 for converting an output of the ADC 32 to an analog signal; a clamping voltage control switch 331 (SW10); a resistive element 332 for setting a time constant; and a capacitive element 333. The feedback clamping voltage Vclp is transmitted to the second addition switch circuit 34 (SW4) via the voltage follower amplifier 39 and is transmitted via the switch circuit 34 to the inversion output terminal OUTN of the differential amplifier 300.

Pages 23 and 24, the paragraph bridging these pages from page 23, line 12 to page 24, line 22, replace the bridging paragraph with:

Fig. 8 shows an example of the operation timing of the circuit shown in Fig. 7. The state of the feedback clamping voltage Vclp is determined in the reference period by the clamping voltage control switch 331 (SW10) and is maintained in the following video period. In the video period, the switches SW3 and SW4 are put in the on state from the reset period T1 to the feedthrough period T2, so that the voltage VRT is obtained at both input terminals of the differential amplifier 300 and the noninversion output terminal OUTP and the inversion output terminal OUTN of the differential amplifier 300 are reset to the voltage VRT and the feedback clamping voltage Vclp. In parallel with the resetting operation, an output voltage of the CCD image pickup device 2 is applied to the sampling capacitive element 301 and the voltage V1 is applied to the sampling capacitive element 302 via the switch SW1, so that charges corresponding to each of the applied voltages are accumulated in each of the sampling capacitors 301 and 302. The difference between the voltage of the sampling capacitor 301 and the voltage of the sampling capacitor 302 in the state (or the output of the differential

amplifier with respect to the difference) can be regarded as a signal voltage corresponding to the black level. When the operation shifts to the charge signal output period T3, the potential of the noninversion input terminal (+) of the differential amplifier 300 is changed in accordance with the change in the output signal CDSIN of the CCD image pickup device 2. In the change amount, the offset voltage of the CCD image pickup device 2 is also included. At this time, the switch SW2 is turned on and the potential of the noninversion terminal (-) of the differential amplifier 300 is changed only by an amount of the offset cancelling voltage Voft. The offset voltage applied to the noninversion input terminal (+) of the differential amplifier 300 is therefore cancelled out by the offset cancelling voltage Voft applied to the inversion input terminal (-). Consequently, the offset voltage component in the CCD image pickup device 2 is eliminated or reduced from the output of the differential amplifier 300.

Pages 26 and 27, the paragraph bridging these pages from page 26, line 11 to page 27, line 6, replace the bridging paragraph with:

Fig. 11 shows a second example of the offset cancelling means. In Fig. 11, the offset cancelling voltage generating

circuit 36 comprises a sample and hold circuit 381 for sampling a clamping voltage Vclp generated by the feedback clamping voltage generating circuit 33; and an inverting amplifier 382 for generating a voltage obtained by adding a voltage V1 to the offset cancelling voltage Voft by a difference voltage between the voltage signal sampled by the sample and hold circuit 381 and a reference voltage signal Vref3 (theoretical clamping voltage). An output of the inverting amplifier 382 is selectively applied to the input stage of the CDS 30 via the second addition switch circuit 37. A resistive element 383 is coupled between an output of the sample and hold circuit 381 and an inverting input terminal (-) of the inverting amplifier 382, and a capacitive element 384 is coupled between the inverting input terminal (-) and the output of the inverting amplifier 382. The other configuration in Fig. 11 is similar to that of Fig. 6. The circuit blocks having the same function are designated by the same reference numerals and its detailed description is omitted here. The offset cancelling means shown in Fig. 11 can automatically cancel the offset voltage by the feedback control in a manner similar to Fig. 6. Consequently, the feedback voltage control amount can be further reduced and the voltage can be accordingly decreased. A change with time in

the temperature characteristic of the offset voltage or the like can be also cancelled.